

Time-aware Redbox Switch In compliance with IEC 61850-3



- Intelligent device that integrates advanced field-proven technology for non-packet-loss redundant Ethernet, sub-microsecond synchronization and cybersecurity.
- Able to merge the whole LAN with redundant networks, to interconnect PRP and HSR networks and to extend HSR rings via QuadBox operation.
- In compliance with IEC 61850-3 / IEEE 1613.
- Ports number can be adapted to customer needs.
- Completely secure and reliable infrastructure.

## **Selection & Ordering data SIC-R**

## SIC-R

Redbox Switch				
0		PORTS 1x 10/100/1000Base-TX Ethernet copper port (Console/Service/Security) + 4x SFP Cages for 10/100/1000Base-TX Ethernet copper or 100Base- FX/1000Base-X fiber		
2		1x 10/100/1000Base-TX Ethernet copper port (Console/Service/Security) + 6x 10/100/1000Base-TX Ethernet copper port + 2x SFP Cages for 10/100/1000Base-TX Ethernet copper or 100Base-FX/1000Base-X fiber		
	0 1 2	POWER SUPPLY 9-26 Vdc 48 Vdc 125 Vdc		

## Example of ordering code:

0	2	SIC R 0 2
SIC	C-R	



## **Technical parameters SIC-R**

	Multiple PTP Tri-speed Ethernet ports
	Zero-Packet-Loss redundancy modes:
	» IEC 62439-3 v3 Clause 5 "High-availability Seamless Redundancy (HSR)"
	Modes: H, N, T, U, X, HSR-SAN, PRP-HSR, HSR-HSR
	» EC 62439-3 v3 Clause 4 "Parallel Redundancy Protocol (PRP)"
Communication Interfaces	Modes: Duplicate discard, duplicate accept, transparent reception, PRP-HSR t
	Optional modes:
	» IEC 62439-2 Clause 5 "Media Redundancy Protocol (MRP)"
	» "Device Level Ring (DLR)" for Ethernet IP » RSTP IEEE802.1w
	VLAN support and Ethernet type based or IEEE 802.1P Traffic prioritization
	Cut-through and Store&Forward switching capability
	IEEE 1588-2008 PTPv2. Optional IRIGb Master/Slave bridge
	Modes: Transparent Clock, Ordinary Clock, Boundary Clock
Synchronization	Profiles: Default, Power, IEC 61850-9-3,AS
c, non chizadon	IEEE 1588 Stateless Transparent Clock P2P mode to support
	IEEE 1588 PRP/HSR redundant networks merging
Other interfaces (not available in	Xilinx Zynq FPGA with embedded dual-core ARM9 processor
all models)	1GB DDR3 RAM Memory
	Linux Operating System
	Optional support for IEC 62351-6 wire-speed cryptography
	Security infrastructure for IEC 62351-9 Key Exchange facilities
	AES 256, HMAC and RSA hardware engines for software and firmware encryption, authentication and signature
	Secure boot
	System Level audited security (OS & Applications)
Security	Integrated anti-tampering, accelerometers and power consumption measurement sensors to mitigate advanced security attacks
	Ethernet port isolated from switching infrastructure to implement security oriented services (NAT, Firewall, VPN, etc.)
	EEE 802.1X access control for port based and MAC based authentication, $\operatorname{MAC}$
	Port binding and authentication for login security
	Optional internal mirroring port with deep packet inspection capability
	Optional integrated SIEM agent for IDS and Syslogv5 TLS support for distributed SIEMs approach
	IEC 61850-3 / IEEE 1613
	Fanless design and full metal enclosure
	Redundant Power Supply: 6VDC to 36 VDC
Rugged devices	Optional PS: 48VDC / 125VDC
	Operating, temperature.: -40°C to +70°C
	Storage temperature.: -40°C to +85°C
	Optional mounting: DIN rail
	SNMPv3, SSH
	Web-based HTML5-GUI access/configuration
Configuration and management	
Configuration and management	Accessible through HTTP(S)
	Configuration profiles and Firmware updates
	Real-time network monitoring

